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Performance Analyzing of a CMOS Circuit's By Sub Clocking Method

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Abstract: Reducing the power consumed by the device is the emerging trend. The aim of this project is to reduce the leakage current of the circuit by using the Sub Clocking technology. It is the process of switching the circuit by means of partially ON to reduce the power consumption. In this paper there are two modes of operation are implemented.1. Half mode operation, 2. Full mode operation. This mode of operation are implemented in the two designing method. Design-1: pMOS and nMOS are connected at the header side of the standard CMOS circuit.Design-2: pMOS and nMOS are connected at the header side of the standard CMOS circuit. pMOS and nMOS transistor at the header and footer side are refer to be as a Sub Clock control unit. Any one of the transistor is ON for a half mode operation and both the transistor are turn ON for full mode of operation. This will done by using the control signal to the unit.

I. INTRODUCTION

Leakage power can be as dominant as dynamic power, poses a large source of power consumption in digital circuits during the active mode, i.e., when the digital circuit is doing useful work. A number of techniques have been proposed for reducing active leakage power dissipation. To obtain the effective result with reduced power consumption the Sub Clocking is used.

In this paper a proposed technique is called the Sub Clock Controlling (SCC), which is target at low power applications. Minimizing the leakage power of the circuit is done by using a two different mode of operation. Full Operating Mode (FOP), Half Operating Mode (HOM). These two modes of operation can be implemented in a two different way (i.e.) two design methodology.

Design-1: pMOS and nMOS are connected at the header side of the standard CMOS circuit.

Design-2: pMOS and nMOS are connected at the header side of the standard CMOS circuit.

pMOS and nMOS are used as a Sub Clock Control circuit to drive the entire circuit by means of voltage divider method. In design-1 the control circuit is connected at the header side of the circuit to control the entire circuit by divide the given supply voltage (VDD).

Similarly in the second design methodology the Sub Clock Control circuit is placed at the footer side in order to reduce the leakage current through the circuit to ground terminal.

II. PROPOSED SYSTEM

In this paper dynamic power consumption and leakage current problem has been rectified and an improved strategy had been implemented by enhancing all the basic compensation techniques in the above stated projects.

The following are the design developed to reduce the leakage power in cmos circuit during the active mode of operation. By activating the CMOS transistor there will be a shot circuit between the Vdd and ground will happen at the 0.7 voltage switching.

This causes a direct link to ground leakage current will more at the time of switching. In order to reduce the leakage current the sub clocking method is implemented. There are two design method is implemented in order to rectify the problems. Half mode operation is used to avoid the ideal current and full mode operation is used to drive the large capacitance load without using the cascading inverter units.

III. A. DESIGN: 1

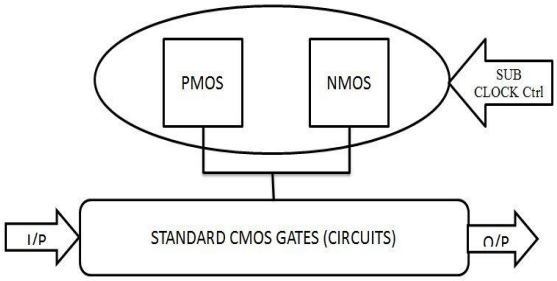

Fig 1:Design-1 block diagram

This design technique the control circuit is placed at the header side of the CMOS circuit.By this process the operating voltage which is given to the circuit is divided into two parts by using the nMOS and pMOS transistor .These transistor are connected in parallel form as shown in the Fig 1.

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Thus the input is given directly to the CMOS circuit and the output is drive directly from the circuit. For half mode power output is control by the sub clock control circuit.(i.e..,)Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the control signal as 0and 1. Similarly the nMOS is switched ON and OFF by using the control signal as 1 and 0.

For a full power operation to drive the large load the control circuitry is switched ON fully mode i.e.., pMOS and nMOS both are in closed circuit. Thus the total power is given to the CMOS circuit.

III B. Design: 2

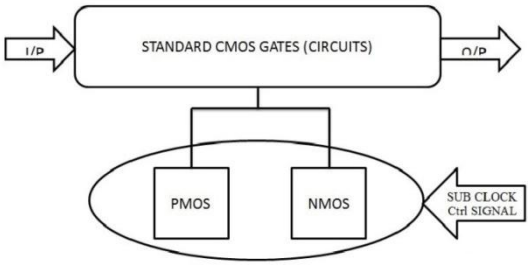

Fig 2: Design-2 block diagram.

This design technique the control circuit is placed at the footer side of the CMOS circuit. By this process the leakage current due to the short circuit between the VDD and GND is reduced by using the nMOS and pMOS transistor .These transistor are connected in parallel form as shown in the Fig 2.

Thus the input is given directly to the CMOS circuit and the output is drive directly from the circuit. For half mode power output is control by the sub clock control circuit. (i.e..,)Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the control signal as 0and 1. Similarly the nMOS is switched ON and OFF by using the control signal as 1 and 0.

For a full power operation to drive the large load the control circuitry is switched ON fully mode i.e.., pMOS and nMOS both are in closed circuit. Thus the total power is given to the CMOS circuit.

IV. IMPLEMENTATION OF THE DESIGN IN BASIC CMOS GATES

The analyzing of a CMOS gates and circuits is done by using the Cadence-Virtuoso tool under the gpdk 180nm technology and the total width of the transistor is fixed at 2µm similarly the finger width is also 2µm ranges.

IV A. NOT gate:

Design: 1 is implemented in the NOT gate transistor level model.This circuit diagram explains how the design is implemented in the standard CMOS gate. By using the control signal to pMOS and nMOS the operation is verified. The output is drive directly from the transistors.

Vdd is given to the circuit is divided into a two parts by nMOS and pMOS transistor and given to the invertor unit. So that depending on the SCC signal the operating power is changed, when pMOS is switched ON and due to the pull up logic the maximum voltage is applied to the circuit and it is operates in the maximum power mode.

Four type of switching is done by pMOS alone ON, nMOS alone ON, both pMOS and nMOS ON or both OFF.

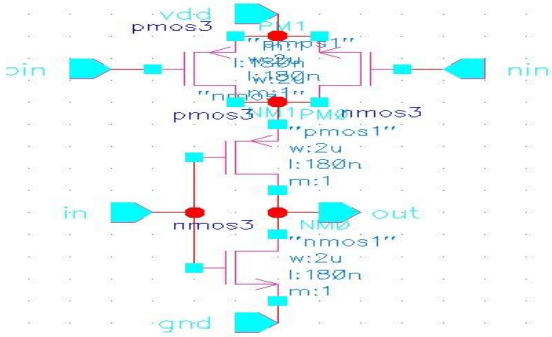

Fig 3:NOT gate with design:1

Design 2: similar to the design 1 technology the SCC is placed in the footer side of the circuit. This is used to block the short circuit between the vdd and gnd,thus it reduce the leakage current of the circuit.

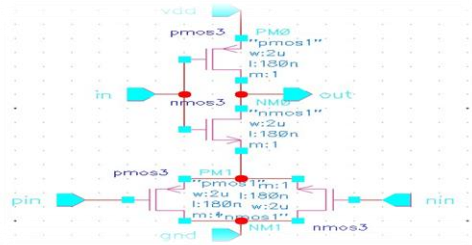

Fig 4: NOT gate with design:2

IV B.EX-OR gate:

Design:1 is implemented in the EX-OR gate transistor level model.

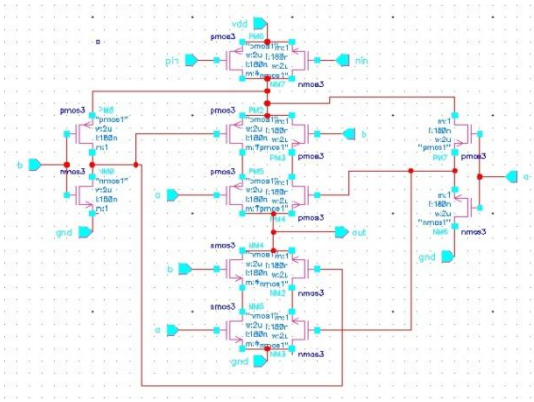

Fig 5: EX-OR gate with design:1

In this circuit the EX-OR gate is controlled by the sub clock control circuit at the header side of the circuit.The supply voltage given to the circuit is control by the control signal given to the CMOS gate. Similarly these design is implemented basic gates and also in various circuits and the power is calculated using the Cadence tool. The transition power is calculated by using the tranpowin the browser window similarly the total power consumption is done by using the calculator—average (get data). By this the overall power is tabulated and checked.

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V. POWER OUTPUTS OF CMOS GATES

V A. Comparison table

S.NO	CMOS gates	Design 1Power in micro watts	Design2Power in micro watts
1	NOT gate	1332	130.82
2	EX-OR gate	107.13	156.92
3	AND gate	118.92	145.7
4	OR gate	87	134.4
5	NOR gate	76.72	96.99
6	NAND gate	111.32	141.7

VI. IMPLEMENTATION OF THE DESIGN IN CMOS CIRCUITS GATES

Designing a SCC circuit the basic gates which is designed with the SCC unit is used to analyze the performance (i.e..,) power consumption of the SCC based CMOS circuit.

VI A Full Adder design using SCC

Full adder contain a 3 inputs(ex:a,b,cin) and 2 outputs(ex:sum,carry).By using the SCC extra two inputs are used (ex:pin,nin)as shown in Fig 6.

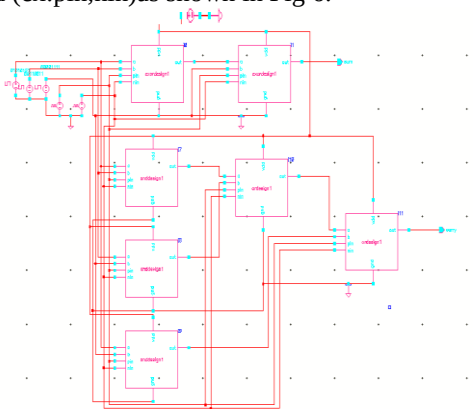

Fig 6: Full Adder with SCC design:1 gates

Power consumption is depending on the switching of the SCC in the gates. Instead of total shutdown the circuit we can make it ideal by off both the pMOS and nMOS in the SCC unit.

VI B Carry Look Ahead Adder design using SCC

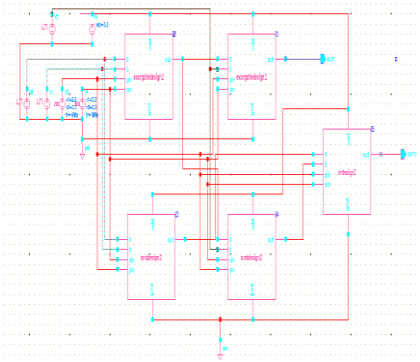

Fig 7: Carry Look Ahead Adder with SCC design:2 gates

Here the CLAA is designed using the SCC design2 gates as shown in the fig.., 7.The SCC of all the gates are combined in a single lined and input is given as common. Depending on the switching the operating power is changed.

VI B(i) Bough-wooley multiplier design using SCC

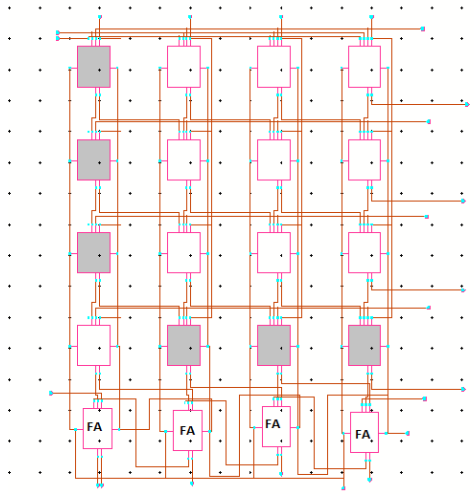

Fig 8: 4 x 4 Bough-wooley multiplier with design 1 gates

BWM is designed with Grey cell and White cell, here the cells are designed by using the SCC gates and implemented with either design 1 or design 2 logic as shown in fig 8

VI B(ii) Bough-wooley multiplier design symbol using SCC

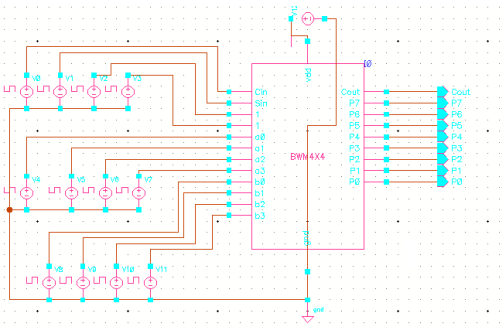

Fig 8: 4 x 4 Bough-wooley multiplier symbol with design 1 gates

BWM contain large number of cells in order to avoid collision the schematic is converted to a symbol and the analyzing is done in the Virtuoso tool.

VII. POWER COMPARISON OF CIRCUITS USING SCC

S.NO	CMOS circuit	Ideal circuit power in milli watts	Design 1 Power in micro watts	Design2 Power in micro watts
1	FA	1.215	79.81	78.56
2	CLAA	915.3	66.79	67.69

FUTURE WORK

Possible future improvements are identify the other technology to further reduce the power consumption of the

circuit without affecting the performance. Analyzing the circuit by varying the nm and also the number of switching with different bits. This technique is implement at different level using Cadence tool implement and simulation output.

CONCLUSION

This paper has proposed a power gating technique that reduces leakage power during the active mode for low performance energy-constrained applications by power gating combinational logic within the clock period. Rather than shutting down completely, symmetric virtual rail clamping was proposed to reduce wake-up power mode transition energy cost. The work proposed in this paper can be considered as an orthogonal approach to the recently proposed sub threshold technique for maximizing energy efficiency when operating at low performance. The sub threshold technique enables realization of minimum energy computation by scaling the supply voltage below Vth until a minimum energy point is found where dynamic energy equals leakage energy per operation.

Due to the aggressively scaled supply voltage, the technique comes at a cost of performance makingit suitable for low performance, energy-constrained applications.

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